UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,034	12/27/2001	Kenneth C. Creta	10559-639001 / P12351	9181

20985 7590 04/04/2005

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,034	CRETA ET AL.	
	Examiner	Art Unit	
	Midys Inoa	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 9-10, filed on December 23rd, 2004, with respect to the rejection(s)of claim(s) 1-11, 13-19, 21-26, and 28-33 under 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Johnson et al. (2003/0084253) in view of Ebner et al (2003/0105929).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim1, 2, 4-8, 10, 11, 13-17, 29-32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (US 2003/0084253) in view of Ebner et al. (2003/0105929).

Regarding Claims 1-2, 34, Johnson discloses a computer system comprising: a cache (Figure 1) including cache lines to store data (lines 0-3 of data section 106), at least a portion of the data to be written to main memory (when a cache line is evicted, it is copied to or written to main memory, paragraph 006), and an eviction mechanism (state machine 116, Figure 1 and paragraph 0010) to evict data stored in one of the cache lines (cache line not accessed or changed... may be preemptively evicted) based on validity state information (age bit in second logical state) associated with the data stored in the cache line, the eviction mechanism to send evicted data to the main memory (when a cache line is evicted, it is copied to main memory,

paragraph 006). Johnson does not disclose each of a subset of the cache lines having multiple portions and validity information that indicates the status of the data in respective portion in the cache line. Ebner discloses Valid Portion bits 211 (see Figure 2) indicating which part of the data line is valid (page 2, paragraph 25). The Valid portion bits 211 reflect the validity of the portions (multiple portions) of the cache line (page 3, paragraph 29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the eviction process of Johnson to evict cache lines based on the valid portion bits of Edner, since giving the system to ability to identify invalid portions of a cache line allows the system to be more precise in its determination of what valid resources are available for use, thus adding flexibility to the manner in which the cache is accessed (Ebner, Abstract).

Regarding Claim 4, Johnson discloses the system further comprising a storage (tag section 108) storing validity bits (age-bits) that track the validity of respective portions of the cache line (paragraph 0023).

Regarding Claim 5, Johnson discloses the system in which the validity bits are set to a predefined value (corresponding age bit is set to a first logical state, paragraph 0010) to indicate that the respective portion has been written in full in one write transaction.

Regarding Claim 6, Johnson discloses the system in which the eviction mechanism (state machine) is to evict the cache line when the validity bits all have the predefined value (second logic state, paragraph 010).

Regarding Claim 7, Johnson discloses the system in which the eviction mechanism (state machine) is to evict the data even if the cache is not full and data in other cache lines is not being

evicted at the same time (lines are evicted when the age bits are in a second logical state. It is not dependent on the cache being full or on other cache lines being evicted, see paragraph 010).

Regarding Claim 8, Johnson discloses the system further comprising the main memory to store the data evicted by the eviction mechanism (paragraph 0006). Since when data is evicted from a cache, it is copied to the main memory; the main memory must store the evicted data.

Regarding Claim 10, Johnson discloses a computer system comprising: cache lines to store bytes of data that correspond to consecutive addresses in a main memory (Figure 1, lines 0-3, data section 106), at least a portion of the data to be written to the main memory (data is written to main memory when evicted, paragraph 006), each cache line corresponding to a group of validity bits (age bits, paragraph 0010), each of the validity bits tracking a portion of the cache line and being set to a predefined value when the tracked portion of the cache line is fully written in one write transaction(set to a first logical state); and an eviction component to evict the bytes of data stored in one of the cache lines when the group of validity bits corresponding to the cache line are all set to the predefined value (second logical state), the eviction component to send the evicted data to the main memory (evicted data is copied to main memory, paragraph 006). Johnson does not disclose each of a subset of the cache lines having multiple portions and validity information that indicates the status of the data in respective portion in the cache line. Ebner discloses Valid Portion bits 211 (see Figure 2) indicating which part of the data line is valid (page 2, paragraph 25). The Valid portion bits 211 reflect the validity of the portions of the cache line (page 3, paragraph 29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the eviction process of Johnson to evict cache lines based on the valid portion bits of Edner, since giving the system to ability to identify invalid

portions of a cache line allows the system to be more precise in its determination of what valid resources are available for use, thus adding flexibility to the manner in which the cache is accessed (Ebner, Abstract).

Regarding Claim 11, Johnson discloses the computer system in which cache lines are disposed within a write cache memory of a computer chipset (See Figure 1).

Regarding Claims 13-14, Johnson discloses the method of a computer system comprising: receiving write transactions associated with data to be written to a main memory wherein the write transactions into the cache are received when a cache miss occurs and the missed data is written to the cache memory, assuming the this data will be accessed again soon (paragraph 006); storing the data into portions of a single cache line of a cache, and evicting the write data from the cache line when the cache line is full of data (if a cache is full, a new line must replace an existing line... if the replaced line is dirty, the line must be evicted) according to stored validity information (dirty bit). The evicted data is copied to the main memory. Johnson does not disclose each of a subset of the cache lines having multiple portions and validity information that indicates the status of the data in respective portion in the cache line. Ebner discloses Valid Portion bits 211 (see Figure 2) indicating which part of the data line is valid (page 2, paragraph 25). The Valid portion bits 211 reflect the validity of the portions of the cache line (page 3, paragraph 29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the eviction process of Johnson to evict cache lines based on the valid portion bits of Edner, since giving the system to ability to identify invalid portions of a cache line allows the system to be more precise in its determination of what valid

resources are available for use, thus adding flexibility to the manner in which the cache is accessed (Ebner, Abstract).

Regarding Claim 15, Johnson discloses the method further comprising setting validity bits to a predefined value when respective portions of the cache line is written in full with write data (first logic state, paragraph 0010).

Regarding Claims 16 and 17, Johnson discloses the method in which the write transactions sent from an input/output device write a first number of data bytes to one of the cache lines. Since the system of Johnson is that of a common computer system, the system must inherently be connected to an input/output device given that a system such as this system is usually connected to a keyboard or mouse (input/output device). It is known that a user has the ability to create files through the use of a keyboard and mouse and such files could be the generated data that is stored in the cache. The eviction component (state machine) evicts a second number of data bytes (data bytes with age-bits in a second logical state, paragraph 0010) in one eviction operation, the first number being less than the second number. The first number of data that needs to be written to the cache must be smaller (or equal in size) to the evicted data since the evicted data can be evicted in order to make room to store the first data (paragraph 006).

Regarding Claims 29-31, Johnson discloses the method of claims 1, 10, 13, 18, and 22 in which writing the data into the cache memory comprises writing the data into the cache memory complying with a cache coherent protocol (paragraph 005).

Regarding Claim 32, Johnson discloses the method of claim 13, further comprising reading a segment of data from the main memory if the write data to be written to the main

memory do not correspond to a cache line address of the cache line, a portion of the segment of data having the same addresses as the data to be written to the main memory. Data is read from main memory when a cache miss occurs (data does not correspond to a cache line), the read data is then written onto the cache, and cache data is evicted to main memory to make room for more data in the cache (paragraph 006).

4. Claims 18-19, 21-23, 28, and 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (US 2003/0084253) in view of Percival (US 2004/0186958).

Regarding Claim 18, Johnson discloses a computer apparatus comprising: a computer chipset comprising a cache memory to store write data (Figure 1) and a mechanism (state machine) to evict the write data from the cache memory when a set of predefined conditions are met (age bits in second logical state, paragraph 010). Johnson evicts the write data from the cache when the cache line is full of data according to stored validity information (dirty bit). The evicted data is copied to the main memory. Johnson does not disclose a cache memory to store data from an input/output device. Percival discloses a cache that caches data from at least one I/O device (Abstract and Claim 37). Since the system of Johnson is that of a common computer system, the system must inherently be connected to an input/output device given that a system such as this system is usually connected to a keyboard or mouse (input/output device), therefore, it would have been obvious to one of ordinary skill in the art to allow the cache to store I/O data as done in Percival's invention since it is known that a user has the ability to create files through the use of a keyboard and mouse (I/O device) and such files are the generated I/O data that is stored in the cache. Additionally, the write data that needs to be written to the cache must be of

smaller or equal in size to the evicted data since the evicted data is evicted in order to make room to store the first data (paragraph 006).

Regarding Claim 19, Johnson discloses the apparatus in which the cache memory also stores additional write data sent from an additional input/output device where the additional device can be one of multiple processors in a multiprocessor system (paragraph 004), and the mechanism also to evict the additional write data from the cache memory when the set of predefined conditions are met (age-bits set to a second logical state, paragraph 010).

Regarding Claim 21, Johnson discloses the apparatus in which write data is combined so that the number of eviction operations performed to evict the write data from the cache memory is less than the number of write transactions (see paragraph 006 and 010). Johnson does not teach an input/output device initiating write transactions to send the write data to the cache. Percival discloses a cache that caches data from at least one I/O device (Abstract and Claim 37). Since the system of Johnson is that of a common computer system, the system must inherently be connected to an input/output device given that a system such as this system is usually connected to a keyboard or mouse (input/output device), therefore, it would have been obvious to one of ordinary skill in the art to allow the cache to store I/O data as done in Percival's invention since it is known that a user has the ability to create files through the use of a keyboard and mouse (I/O device) and such files are the generated I/O data that is stored in the cache. Additionally, the write data that needs to be written to the cache must be of smaller or equal in size to the evicted data since the evicted data is evicted in order to make room to store the first data (paragraph 006).

Regarding Claim 22, Johnson discloses the method of a computer system comprising: writing the data into a cache memory (Figure 1); evicting the data from the cache memory (when the age-bits are on second logical state, paragraph 010); and writing the data into a main memory (evicted data is copied into main memory, paragraph 006). Johnson does not teach initiating write transactions by an input/output device to write data. Percival discloses a cache that caches data from at least one I/O device (Abstract and Claim 37). Since the system of Johnson is that of a common computer system, the system must inherently be connected to an input/output device given that a system such as this system is usually connected to a keyboard or mouse (input/output device), therefore, it would have been obvious to one of ordinary skill in the art to allow the cache to store I/O data as done in Percival's invention since it is known that a user has the ability to create files through the use of a keyboard and mouse (I/O device) and such files are the generated I/O data that is stored in the cache. Additionally, the write data that needs to be written to the cache must be of smaller or equal in size to the evicted data since the evicted data is evicted in order to make room to store the first data (paragraph 006).

Regarding Claim 23, Johnson discloses the method in which the cache memory contains cache lines configured to store data, each cache line corresponding to consecutive addresses in the main memory (Figure 1, data section 106, lines 0-3). From Figure 1, it is visible that if 106 is one single section of data, and lines 0-3 represent that data, lines 0-3 represent consecutive addresses.

Regarding Claims 28 and 33, Johnson discloses the method in which writing the data into the cache memory comprises writing the data into the cache memory complying with a cache coherent protocol (paragraph 005).

5. Claims 24-26 rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (US 2003/0084253) in view of Percival (US 2004/0186958) further in view of Ebner et al. (2003/0105929

Regarding Claim 24, Johnson in view of Percival discloses the method of Claim 23 wherein each cache line has multiple portions (a cache line is typically divided into multiple words, paragraph 003). Johnson teaches a single validity bit (age-bit) being used to determine if eviction is necessary. Johnson in view of Percival does not teach each portion corresponding to validity bit that tracks the status of the corresponding portion. Ebner discloses Valid Portion bits 211 (see Figure 2) indicating which part of the data line is valid (page 2, paragraph 25). The Valid portion bits 211 reflect the validity of the portions (multiple portions) of the cache line (page 3, paragraph 29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the eviction process of Johnson to evict cache lines based on the valid portion bits of Edner, since giving the system to ability to identify invalid portions of a cache line allows the system to be more precise in its determination of what valid resources are available for use, thus adding flexibility to the manner in which the cache is accessed (Ebner, Abstract).

Regarding Claim 25, Johnson in view of Percival further in view of Ebner disclose the method in which the validity bit (Johnson, age bit) is set to a predetermined value responsive of the number of bytes of data written into the corresponding portion (first logical state, paragraph 010).

Regarding Claim 26, Johnson discloses the method in which the evicting the data from the cache memory comprises evicting the data when the validity bit (age-bit) corresponding to a

cache line is set to a predefined value (second logical state, paragraph 010). Johnson in view of Percival does not teach each portion corresponding to validity bit that tracks the status of the corresponding portion. Ebner discloses Valid Portion bits 211 (see Figure 2) indicating which part of the data line is valid (page 2, paragraph 25). The Valid portion bits 211 reflect the validity of the portions (multiple portions) of the cache line (page 3, paragraph 29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the eviction process of Johnson to evict cache lines based on the valid portion bits of Edner, since giving the system to ability to identify invalid portions of a cache line allows the system to be more precise in its determination of what valid resources are available for use, thus adding flexibility to the manner in which the cache is accessed (Ebner, Abstract). In changing the single validity bit of Johnson for the multiple validity bits of Ebner, it would be necessary for all the validity bits to have an invalid value for eviction to occur.

6. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (US 2003/0084253) in view of Ebner et al. (2003/0105929) further in view of Percival (US 2004/0186958)

Regarding Claim 9, Johnson in view of Ebner discloses the system of Claim 1. Johnson in view of Ebner does not teach the data being generated by an input/output device and stored in a cache. Since the system of Johnson is that of a common computer system, the system must inherently be connected to an input/output device given that a system such as this system is usually connected to a keyboard or mouse (input/output device). It is known that a user has the ability to create files through the use of a keyboard and mouse and such files could be the generated data that is stored in the cache. Percival discloses a cache that caches data from at

least one I/O device (Abstract and Claim 37). Since the system of Johnson is that of a common computer system, the system must inherently be connected to an input/output device given that a system such as this system is usually connected to a keyboard or mouse (input/output device), therefore, it would have been obvious to one of ordinary skill in the art to allow the cache to store I/O data as done in Percival's invention since it is known that a user has the ability to create files through the use of a keyboard and mouse (I/O device) and such files are the generated I/O data that is stored in the cache. Additionally, the write data that needs to be written to the cache must be of smaller or equal in size to the evicted data since the evicted data is evicted in order to make room to store the first data (paragraph 006).

7. Claims 12 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (US 2003/0084253) in view of Ebner et al. (2003/0105929) further in view "Cache Consistency Protocol" by Peter G. Sassone.

Johnson in view of Ebner discloses the system of claims 29 and 30 with a cache coherency protocol comprising a MSI protocol (Johnson). Johnson does not teach a modified-exclusive-invalid (MEI) protocol or a modified-exclusive-shared-invalid (MESI) protocol. "Cache Consistency Protocol" by Peter G. Sassone discloses a MESI protocol, which improves performance over a MSI protocol (See page 2). It would have been obvious to change the MSI protocol of Johnson et al. to the MESI protocol of Sassone since adding the Exclusive state to the protocol provides a coherency protocol with a better performance and lower average clocks per instruction per processor (see page 4).

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (US 2003/0084253) in view of Percival (US 2004/0186958) further in view "Cache Consistency Protocol" by Peter G. Sassone.

Johnson in view of Percival discloses the system of claims 29 and 30 with a cache coherency protocol comprising a MSI protocol (Johnson). Johnson does not teach a modified-exclusive-invalid (MEI) protocol or a modified-exclusive-shared-invalid (MESI) protocol. "Cache Consistency Protocol" by Peter G. Sassone discloses a MESI protocol, which improves performance over a MSI protocol (See page 2). It would have been obvious to change the MSI protocol of Johnson et al. to the MESI protocol of Sassone since adding the Exclusive state to the protocol provides a coherency protocol with a better performance and lower average clocks per instruction per processor (see page 4).

Conclusion

9. The prior art made of record and relied upon is considered pertinent to applicant's disclosure:

1. Percival (US 2004/0186958) A Method and System for Coherently Caching I/O Devices Across a Network.

2. Ebner et al. (US 2003/0105929) Cache Status Data Structure

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 28th, 2005

Midys Inoa
Examiner
Art Unit 2189

MI

Pierre M. Vital
Primary Examiner
Art Unit 2188